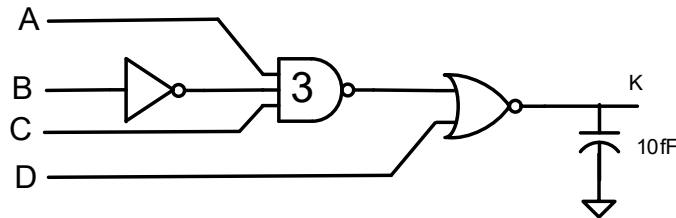


This assignment will not be collected or graded. Even though the problems will not be collected, students are advised to work enough of them to have mastery of the material prior to looking at the posted solutions.

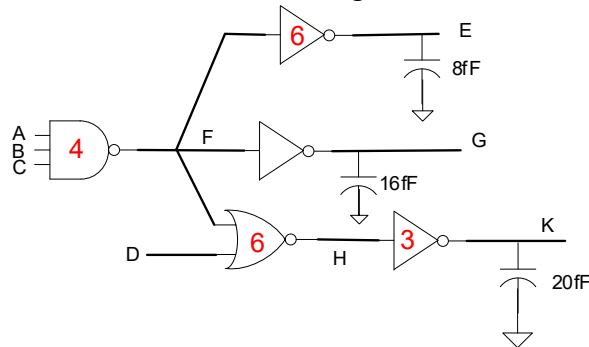
If references to a semiconductor processes are needed beyond what is given in a specific problem or question, assume a CMOS process is available with the following key process parameters;  $\mu_n C_{OX}=100\mu A/v^2$ ,  $\mu_p C_{OX}=33\mu A/v^2$ ,  $V_{TNO}=0.8V$ ,  $V_{TPO}= - 0.8V$ ,  $C_{OX}=4fF/\mu^2$ ,  $\lambda = 0$ ,  $\gamma = 0$ ,  $L_{MIN}=W_{MIN}=0.6\mu$ , and  $V_{DD}=4V$ .

**Problem 1** Determine the propagation delay in terms of  $t_{REF}$  from B to K for the following circuit. Assume all devices sized for equal worst-case rise and fall times. The OD for the gates, if different than 1, are as indicated.



**Problem 2** Assume you are working in a  $0.5\mu$  CMOS process.

- Size the devices in the 3-input NAND gate for an overdrive of 4 and the 2-input NOR gate for an overdrive of 6 with the equal rise/fall sizing strategy. The overdrive factors for the inverters are indicated.
- With this sizing, how does the propagation delay from B to K compare to that of a minimum- sized reference inverter driving an identical 20fF load?

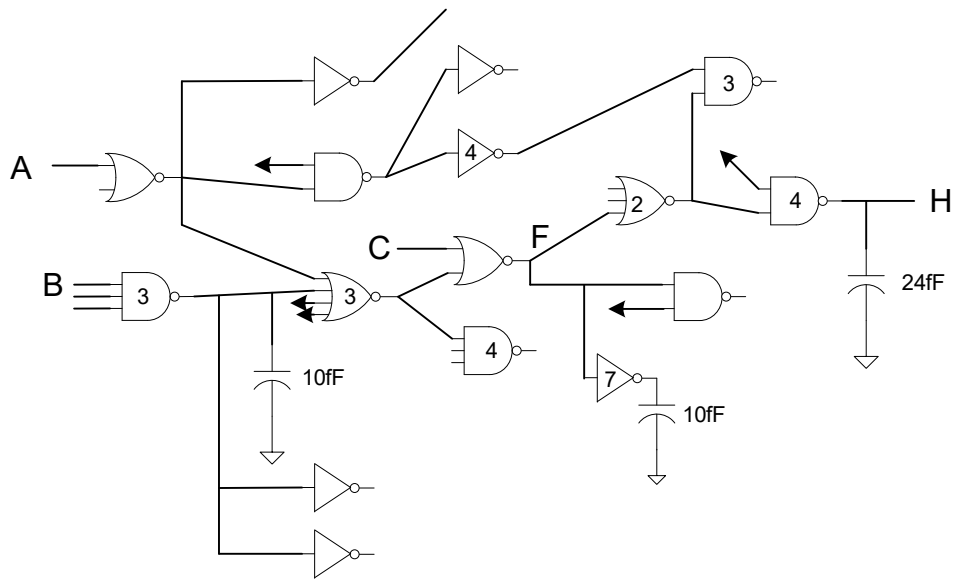


**Problem 3** A segment of a logic block is shown below. Assume the lengths of all devices are  $L_{MIN}$ . Assume all gates are sized for equal worst-case rise and fall times.

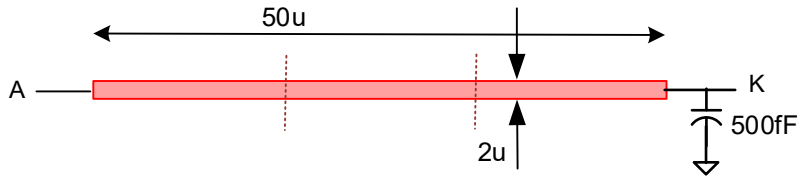
Gates with an overdrive factor that is different than 1 are as indicated by a number on the gate. Assume that the process in which these gates are fabricated is characterized by a minimum length reference inverter with

$$t_{REF}=20ps, C_{REF}=4fF, R_{PDREF}=2.5K, V_{DD}=4V$$

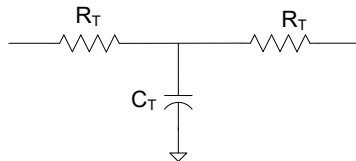
- Determine the worst-case propagation delay from A to F
- Determine the dynamic power dissipation in inverter with OD=4 if A is clocked at 400MHz and the output of this inverter changes on each H-L transition of the A input.
- Repeat part a) if all gates are minimum sized.



**Problem 4** A poly interconnect that is  $2u$  wide and  $50u$  long is used to connect a low impedance signal to a  $500fF$  load. Assume the capacitance density of this poly layer is  $.5fF/u^2$  and the sheet resistance of the poly is  $20\text{ ohms/square}$ .

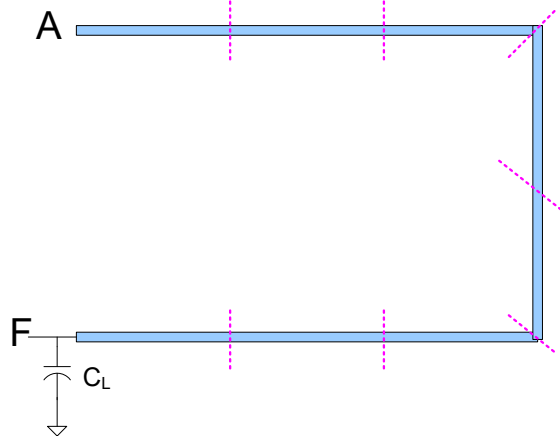


a) If this interconnect is modeled by the series connection of 3 T-connected segments shown, determine the value of the resistors  $R_T$  and the capacitor  $C_T$  in each of these segments.



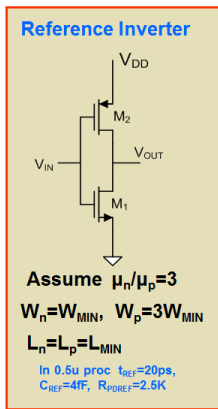
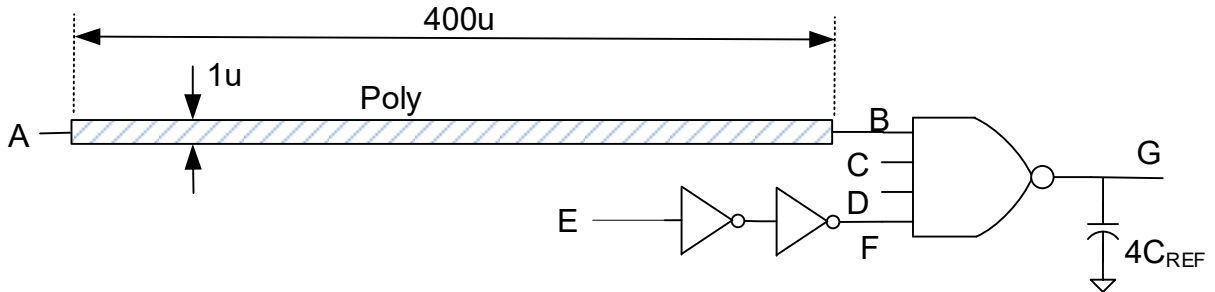
- b) Determine the Elmore delay for driving the output K associated with this interconnect model
- c) Compare the Elmore delay with that obtained with a Spice simulation using the same 3 T-connected segments

**Problem 5** A poly interconnect that is  $2u$  wide is used to connect a low impedance signal at node A to a  $50fF$  load at node F as shown below. The distance between the dashed segments is  $50u$ . Assume the capacitance density of this poly layer is  $.5fF/u^2$  and the sheet resistance of the poly is  $20\text{ ohms/square}$ . Calculate the Elmore delay from A to F using a T-model for each of the  $50u$  segments. Assume  $C_L=100fF$ .



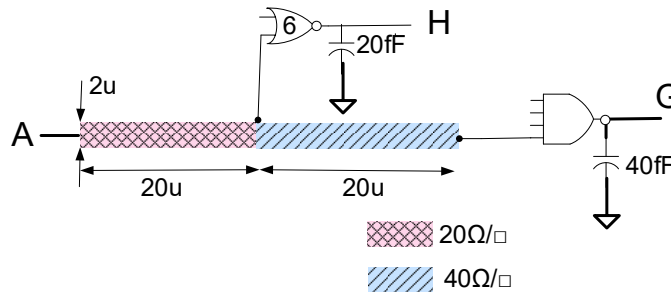
**Problem 6** Assume Poly has a sheet resistance of  $50\Omega/\square$  and a capacitance density to substrate of  $800\text{aF}/\mu\text{m}^2$ . Assume all gates are sized for equal worst-case rise and fall times with  $\text{OD}=1$ . A reference inverter in this process is shown below. Assume the C and D inputs are both a Boolean 1.

- If a low to high input transition occurs simultaneously on the A and E inputs, will the B input or the F input rise first? (Be quantitative in your comparison)
- If the inputs A, C, and D are Boolean 1, calculate the propagation delay ( $t_{\text{HL}}+t_{\text{LH}}$ ) from E to G.



**Problem 7** Assume a process has Poly with two different sheet resistances as shown below. Assume the capacitance density to substrate of both Poly layers is  $800\text{aF}/\mu\text{m}^2$ . Determine the propagation delay from A to G. Assume the gates in the process are characterized by a minimum length reference inverter with

$t_{\text{REF}}=20\text{ps}$ ,  $C_{\text{REF}}=4\text{fF}$ ,  $R_{\text{PDREF}}=2.5\text{K}$ ,  $V_{\text{DD}}=4\text{V}$



**Problem 8** A standard CMOS inverter with  $W_n=10\mu$ ,  $W_p=40\mu$ ,  $L_n=0.6\mu$  and  $L_p=0.6\mu$  is driving a 600fF capacitive load. Assume  $C_{ox}$  for the process is 4fF/ $\mu^2$  and a supply voltage of 4V.

- Determine the dynamic power dissipation in the inverter if the input to the inverter is a 10KHz square wave.
- Repeat a) if  $W_n = W_p = 0.6\mu$
- How fast can the inverter be clocked if the original device sizes are used?

**Problem 9** Determine the energy required to drive a minimum sized static CMOS inverter for a HL followed by a LH transition in a 0.5 $\mu$  CMOS process. From these results, make a prediction on the power level that would be expected in a system with 1 million gates if half of the gates transitioned on each clock cycle and if all of the gates had an input capacitance equal to that of a minimum-sized inverter. Assume the clock of the system is 1.5GHz. Assume the gates in the process are characterized by a minimum length reference inverter with

$$t_{REF}=20ps, C_{REF}=4fF, R_{PDREF}=2.5K, V_{DD}=4V$$

**Problem 10** Determine the power that would be required in the final driver stage of a pad driver needed to drive a 25pF external load at 300MHz. Assume the gates in the process are characterized by a minimum length reference inverter with

$$t_{REF}=20ps, C_{REF}=4fF, R_{PDREF}=2.5K, V_{DD}=4V$$

**Problem 11** Assume a 32-bit data bus needs to go off chip and that the average capacitance on each bit is 4pF. Determine the dynamic power dissipation in the last stage of a pad driver that drives this bus if the clock rate is 800MHz. Assume logic with  $V_H=4V$ ,  $V_L=0V$  is being used and that, on the average, each bit changes once every other clock period.

**Problem 12** Design a pad driver to drive a 32-bit data bus. Assume the load on each bit of the bus is 600fF and that the clock speed for data on the bus is 100MHz. The pad driver should be designed so to minimize the power dissipation in the pad driver while still meeting the 100MHz speed requirement. Assume the gates in the process are characterized by a minimum length reference inverter with

$$t_{REF}=20ps, C_{REF}=4fF, R_{PDREF}=2.5K, V_{DD}=4V$$

**Problem 13.** What is the fastest clock that can be used in a 0.5 $\mu$  process if the clock must drive a 2pF load. Assume a standard pad driver structure is used to drive this load. Assume the gates in the process are characterized by a minimum length reference inverter with

$$t_{REF}=20ps, C_{REF}=4fF, R_{PDREF}=2.5K, V_{DD}=4V$$

**Problem 14** Consider the cascade of 3 inverters with a 50fF load on the last stage. Assume they are designed in a CMOS process characterized by a minimum length reference inverter with

$$t_{REF}=20ps, C_{REF}=4fF, R_{PDREF}=2.5K, V_{DD}=4V$$

- Determine the propagation delay if the devices are sized for equal rise/fall times and all have an overdrive of 1.
- Repeat part a) if all devices are minimum sized
- Determine the total dynamic power dissipation if the input is a square wave of frequency 10MHz if the devices are sized as in part a)
- Repeat part c) if all devices are minimum sized.

**Problem 15** Implement the following Boolean circuit at the transistor level with dynamic zipper logic. Any gate can have at most 3 inputs.

$$F=(ABC+\bar{A}D)\cdot E$$

**Problem 16** Design a ring oscillator that will oscillate at a frequency of 80MHz in the 0.5u CMOS process. Assume a supply voltage of 4V is to be used for the ring oscillator. Assume the gates in the process are characterized by a minimum length reference inverter with

$$t_{REF}=20ps, C_{REF}=4fF, R_{PDREF}=2.5K, V_{DD}=4V$$

**Problem 17** A 5-transistor memory cell is loaded with  $X_D$  when  $\phi$  is high and holds the value of  $X_D$  when  $\phi$  is low. Assume  $M_1, M_2, M_3$  and  $M_4$  all have  $W=1\mu$  and  $L=2\mu$  and the length of  $M_5$  is  $1\mu$ . If a high Boolean signal is 4V and a low Boolean signal is 0V, determine the minimum value of  $W_5$  needed to guarantee that the value of  $X_D$  can be written into the memory cell. Assume the gates in the process are characterized by a minimum length reference inverter with

$$t_{REF}=20ps, C_{REF}=4fF, R_{PDREF}=2.5K, V_{DD}=4V$$

